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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,237	08/27/2003	Chaur-Chin Yang	BHT-3183-53	3764

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EXAMINER	
ROSE, KIESHA L	

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/648,237	YANG ET AL.	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-36,38 and 39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-36 and 38-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the RCE filed 11/19/07.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 25-28,33-34,36 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Giri et al. (U.S. Patent 6,765,152) in view of Jiang et al. (U.S. Publication 2003/0164556).

In re claim 25, Giri discloses a chip module (Figs. 1-4) that contain a substrate (12) having a top surface, bottom surface and a substrate opening extending through the top surface and the bottom surface, a dummy die (18) (interposer) having no electrical function connected to the bottom surface and aligned with the substrate opening, wherein the dummy die has a redistribution layer electrically connected with the substrate having flip chip pads and connecting pads connected by a trace on the top surface of the dummy die below the substrate opening, the connecting pads of the redistribution layer are electrically connected to the substrate, wherein the dummy die has an exposed surface located on the bottom thereof and a chip (22) located in the opening and having a plurality of bumps electrically connected with the flip chip pads of

the redistribution layer. Giri discloses all the limitations except for the dummy die to have a metal thermal-conducting layer directly formed thereon. Whereas Jiang discloses a microelectronic component (Fig. 4) that contains a dummy die (100) being a silicon substrate (interposer) formed with a metal thermal-conducting layer (104) directly formed thereon to substantially cover the exposed surface located on the bottom of the dummy die. The metal thermal-conducting layer is formed to supply electrical connection and act as conductive traces for the interposer. (Paragraph 0041) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Giri by incorporating a metal thermal-conducting layer directly formed on the dummy die to supply electrical connection and act as a conductive trace as taught by Jiang.

In re claim 26, Giri discloses a package body (34) located in the substrate opening and encasing the chip. (Fig. 2)

In re claim 27, Giri discloses the substrate is a printed circuit board. (Column 3, lines 42-46)

In re claim 28, Giri discloses the dummy die has a size larger than a size of the chip. (Figs. 1-2)

In re claim 33, Giri discloses a plurality of top connection pads located on the top surface of the substrate. (Fig. 3, area where wires (52) are connected)

In re claim 34, Giri discloses a plurality of solder balls (14) connected to the bottom substrate surface. (Fig. 2)

In re claim 36, Giri discloses an adhesive tape connecting the dummy die to the bottom surface of the substrate. (Column 5, lines 10-13)

In re claim 39, Giri and Jiang disclose all the limitations except for the metal thermal-conducting layer to be a sputtered metal layer; this limitation is a product by process limitations. A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear. Even though product –by [-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted)."

Claims 29-30 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Giri and Jiang in view of Klein et al. (U.S. Publication 2004/0145051).

In re claims 29 and 35, Giri and Jiang disclose all the limitations except for stacked semiconductor package and pitch size for the flip chip pads. Whereas Klein discloses a semiconductor package (Fig. 9a) that contains a die (12) with a redistribution layer formed thereon with flip chip pads (22) and connecting pads where the flip chip pads have a smaller pitch than the connecting pads and a plurality of stacked semiconductor packages including a plurality of outer terminals (118) connecting the connection pads (52). The package is a stacked semiconductor package in order to form a system. (Page 7, Paragraph 96) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the devices of Giri and Jiang by incorporating a stacked semiconductor package to create a system for electrical connection as taught by Klein.

In regards to claim 30, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the pitch of the flip chip being 150 m, since it has been held that discovering the optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (1980).

Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Giri and Jiang in view of Kikuma et al. (U.S. Patent 6,621,169).

In re claim 31, Giri and Jiang disclose all the claimed limitations except for bonding wires connecting the redistribution layer to the substrate. Whereas Kikuma discloses a stacked semiconductor device (Fig. 25) that contains a substrate (108) and a chip with a redistribution layer (114) formed thereon where the redistribution layer and substrate are connected by bonding wires (116). The substrate and redistribution layer

are connected by bonding wires to form an electrical connection between the two. (Column 17, lines 60-64) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the devices of Giri and Jiang by incorporating the redistribution layer and substrate to be connected by bonding wires to form an electrical connection between the two as taught by Kikuma.

Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Giri and Jiang in view of Koopmans (U.S. Publications 2004/0035840).

In re claim 32, Giri and Jiang disclose all the limitations except for bumps bonding the connecting pads of the redistribution layer to the substrate. Whereas Koopmans discloses a flip chip (Fig. 1a) that contains a substrate (34) and a redistribution layer (21) with connecting pads (20) and bumps (26) that bond the connecting pads of the redistribution layer to the substrate. The bumps are formed between the connecting pads of the redistribution layer and the substrate to enable electrical interconnection to a package (redistribution layer and substrate). (Page 1, Paragraph 7) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the devices of Giri and Jiang by incorporating bumps between the connecting pads of the redistribution layer and the substrate to enable electrical interconnection to a package (redistribution layer and substrate) as taught by Koopmans.

Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Giri and Jiang in view of Higgins III (U.S. Patent 5,583,377).

In re claim 38, Giri and Jiang disclose all the claimed limitations except for the substrate to have a stair configuration. Whereas Higgins discloses a semiconductor device (Fig. 2) that contains a substrate (42) with a stair configuration (44) and a chip (13) mounted in the opening of the substrate. The substrate is formed with a stair configuration to help with the manufacturing cost and form a lower profile device. (Column 5, lines 18-20) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the devices of Giri and Jiang by incorporating the substrate to have a stair configuration to help with manufacturing cost and make a lower profile device as taught by Higgins.

Response to Arguments

Applicant's arguments filed 11/19/07 have been fully considered but they are not persuasive. Applicant argues that the Giri reference does not disclose the redistribution layer being electrically isolated from the metal thermal conducting layer. This is erroneous as seen in the Giri reference the dummy dies a tape or interposer with a redistribution layer formed thereon and the Jiang reference is used for the metal thermal conducting layer formed on the bottom of the dummy die. If the dummy die is a tape then there is no electrical function in the die as claimed and the redistribution layer and metal thermal conducting layer would be electrically isolated from each other. Therefore the Giri and Jiang reference disclose the claimed limitations and the rejection stands.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on T-F 8:30-6:00 off Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KLR

/Kiesha L. Rose/

Primary Examiner, Art Unit 2822

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/648,237	YANG ET AL.	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	